System Test Results from LBL

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Description of setup:

- Disk sector with modules
- Electrical services
- Test configuration

Measurement results:

- First studies of module performance before/after sector mounting
- Future plans: inject noise into cooling structure, testing with service panel

Disk Sector Setup

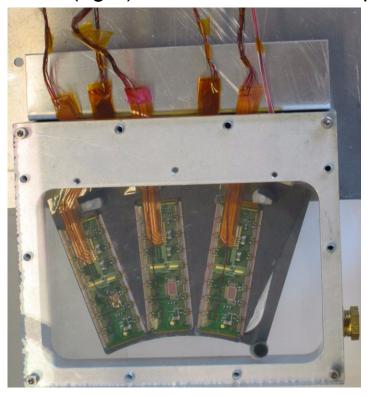
Initial configuration:

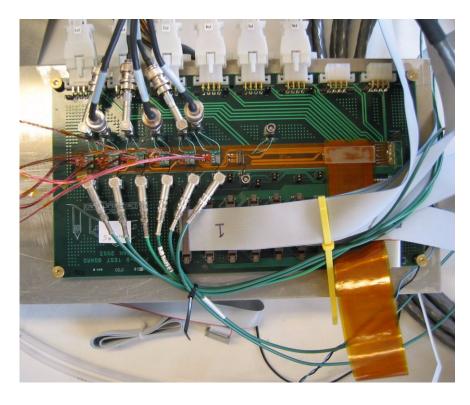
- •During the Feb pixel week, three modules were attached to the top side of a prototype disk sector using CGL adhesive. These modules are LBL_3, LBL_4, and LBL_7.
- •These modules were not mounted with a real module pickup fixture, but rather "by hand" in order to proceed to investigate multi-module electrical issues as rapidly as possible.
- •Extensive measurements were performed on these modules during March.
- •It was observed that both of the AMS modules suffered localized bump damage between the last bench test and the first tests on the sector. This is presumably a result of the improvised tooling.

Final configuration:

- During the May irradiation, three additional modules were mounted on the bottom of the prototype disk sector using SE adhesive. These modules are LBL_13, LBL_14, and LBL_16.
- •These modules were mounted using a reasonable pickup fixture, but the rest of the tooling was not yet close to "production quality"
- •This configuration was briefly tested in early June, and all modules worked well, with no sign of bumping damage.

•Disk sector with six disk modules mounted (left) and connected to PP0 Support board (right) with all services for operation:

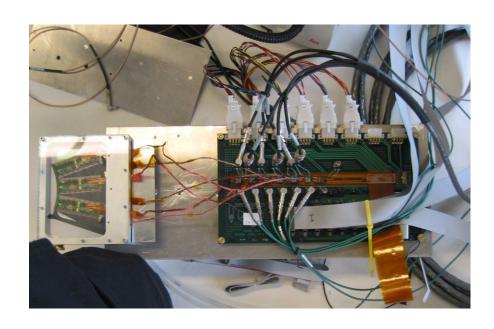


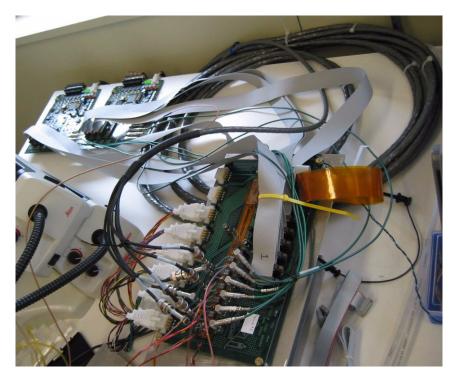


- Five of the disk modules are of the older "pigtailed" variety. LBL_15 and LBL_16 are the new "pigtail-less" variety.
- •The PP0 Support board provides connections for LV, HV, VCal, and the TPCC connections for readout.

Readout setup

•Top three modules were read out out with one TPLL/TPCC. Bottom three modules were read out with a second TPLL/TPCC. However, both TPLL were in the same VME crate, and were read by the same PC. A Desktop Manager (Flash Desktop) was used to provide multiple desktops for running multiple copies (two) of TurboDAQ.



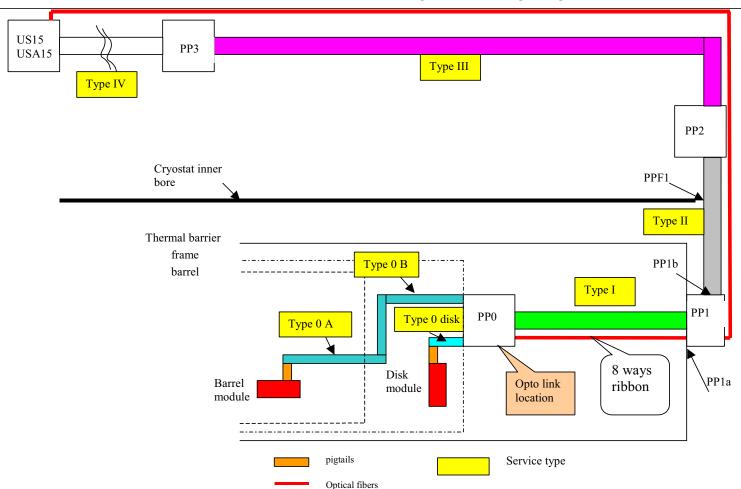


•Major limitation of this arrangement was that, due to the fact that TurboDAQ locks the GUI during scans, it was almost impossible to toggle back and forth between multiple copies of TurboDAQ. Note coiled 12m Type 2 cable in right photo.

- •In addition, even when both versions of TurboDAQ, competition for resources (both CPU and memory, and the VME interface) tended to eliminate any concurrency, and scan steps for the two modules would run in an "interleaved" mode.
- •Could do much better by allocating a second PC to the operation of the system test. Will do this for limited time for additional multi-module interference testing.
- •Of course, the next logical step is to begin trying to read out the disk sector with the ROD. This would provide truly independent operation for different modules at the same time, and would also support operations like multi-module source scans.

Services setup

•Services setup is intended as a realistic electrical representation of the final services scheme, with reasonable wire lengths and gauges.



•PP0 is represented by the PP0 Support board. Type 1 and Type 2 cables are combined into a single 12m cable. Type 3 and Type 4 are combined into a single 140m cable.

Cables:

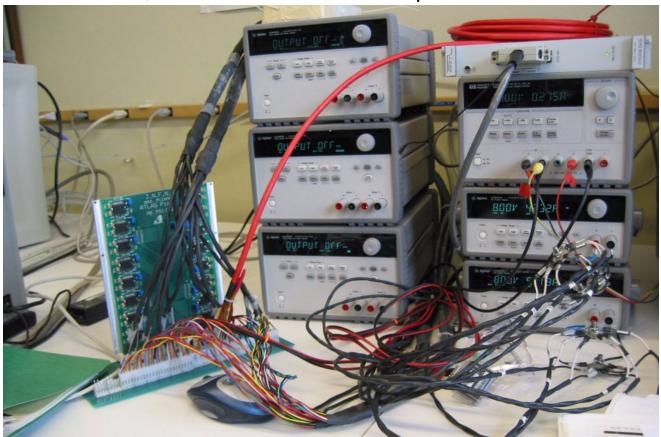




- •On the left are two large rolls for 140m 6-pair AWG16 twisted-pair Type 3 cables (total mass about 100kg), connecting the Agilent LV supplies with the regulator board. One cable is for VDD and one cable is for VDDA.
- •On the right is a roll for 150m 6-pair AWG24 twisted-pair Type 3 cable for the ISEG HV supply. The chosen wire gauge was the smallest with an acceptable voltage rating.

Regulators:

•Used first prototype ST regulator board from Milano. Regulators were operated in remote sense mode, but without "current compensation":



- •In this case, individual 8A supplies were used to power all six modules simultaneously, with one supply providing VDD, and the other VDDA.
- •Used 8V output voltage to conservatively guarantee correct voltage at module.

Low Voltage:

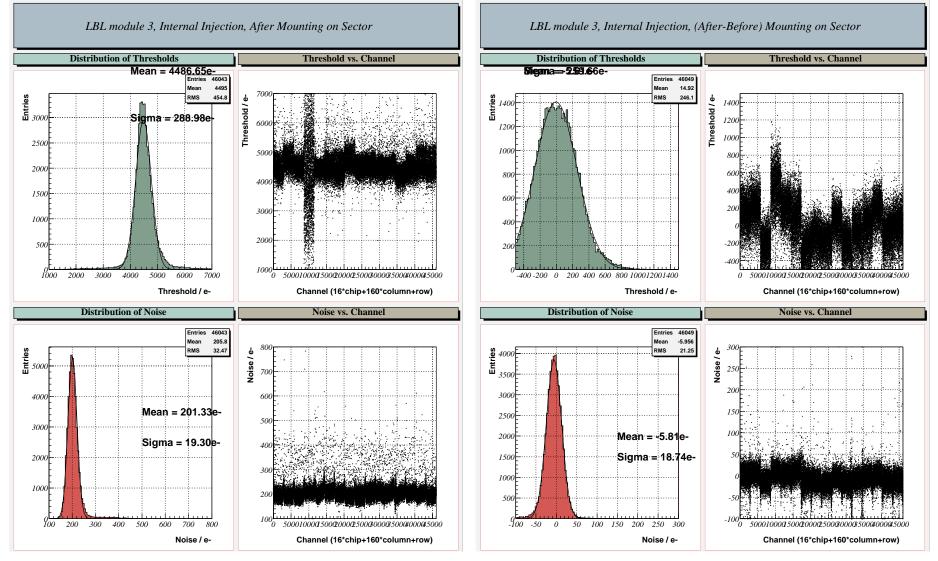
- •Agilent lab supplies used for LV. Have tried multiplicity one (three supply pairs used to operate three modules), multiplicity three (one supply pair for three modules), a mixed multiplicity three for the top three modules and multiplicity one for the lower three modules, and finally, multiplicity six with all modules operating on a single supply pair.
- •Regulator board always supplied one module per channel pair. Multiplicity n was implemented by connecting the long cables together at the supply end, just as it would be with our baseline detector using multiplicity one services and multiplicity up to six power supplies.

High Voltage:

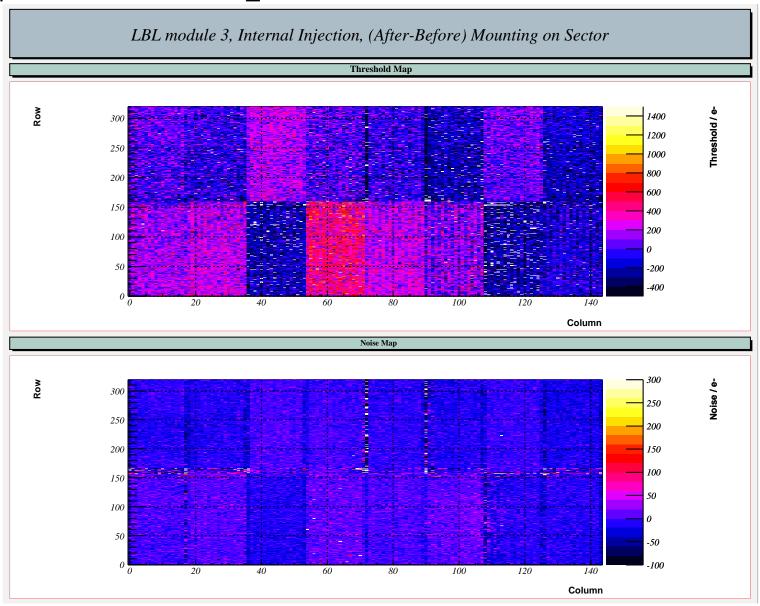
- •A single ISEG supply was used to control the HV, with multiplicity = 1. This was not very realistic, but ganging of HV channels would be difficult due to the complex connector on the ISEG module.
- •The control of the high voltage was implemented in TurboDAQ. Unfortunately, the DLL from the vendor is not reliable, and causes TurboDAQ to crash on a daily basis.

First Measurements:

•Compare threshold scans made with single modules in the lab and with modules mounted on sector. LBL_3 shows similar noise, increased dispersion due to ΔT :

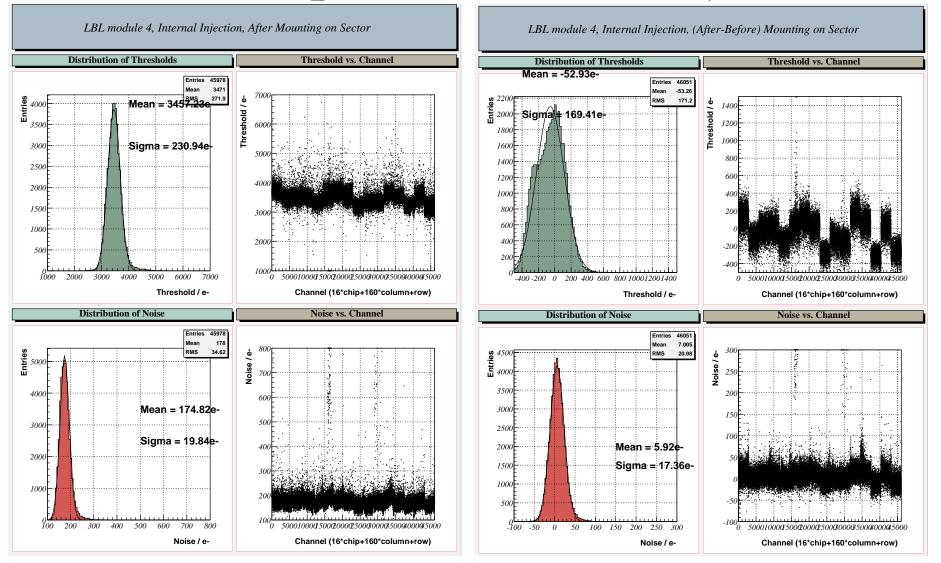


Map of differences for LBL_3:

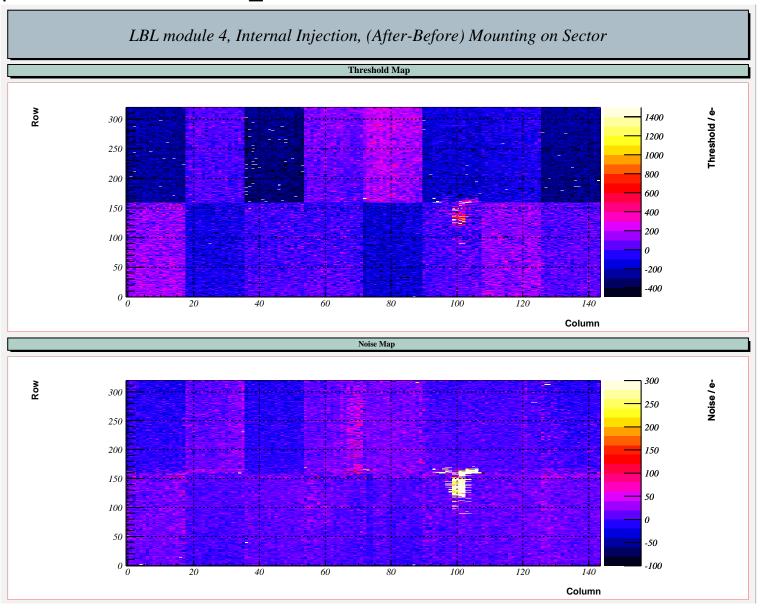


•Differences seen can mainly be attributed to fact that pre-mount scan was in "AntiKill" mode and post-mount scan was in "Stage" mode.

 Compare threshold scans made with single modules in the lab and with modules mounted on sector. LBL_4 shows similar noise, increased dispersion due to ΔT :

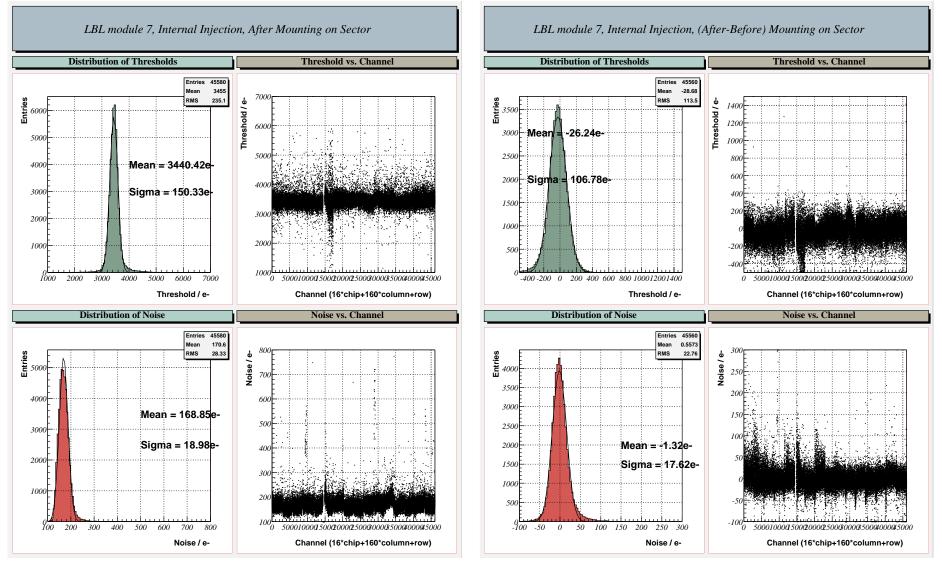


Map of differences for LBL_4:

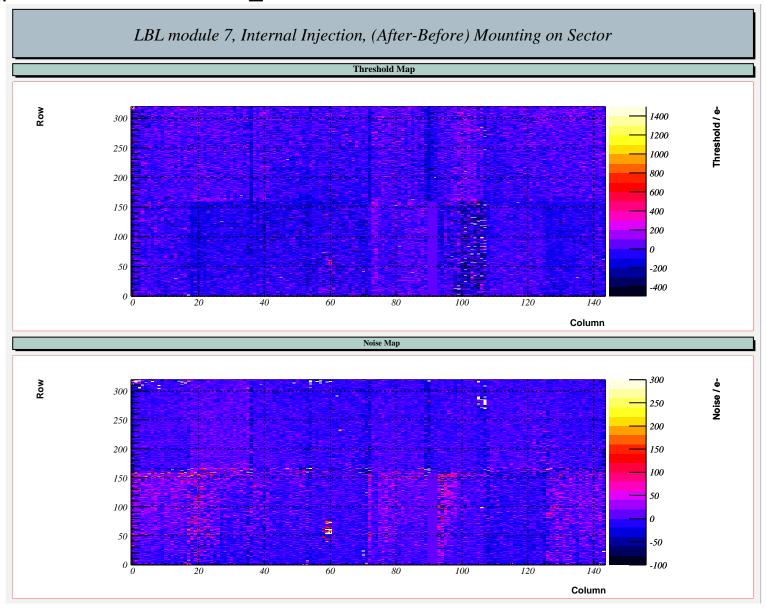


•Major observation is significant bump damage in chips 5 and 10. Crosstalk scans confirm that there are now a large number of merged or almost merged bumps.

•Compare threshold scans made with single modules in the lab and with modules mounted on sector. LBL_7 shows similar noise, increased dispersion due to ΔT :



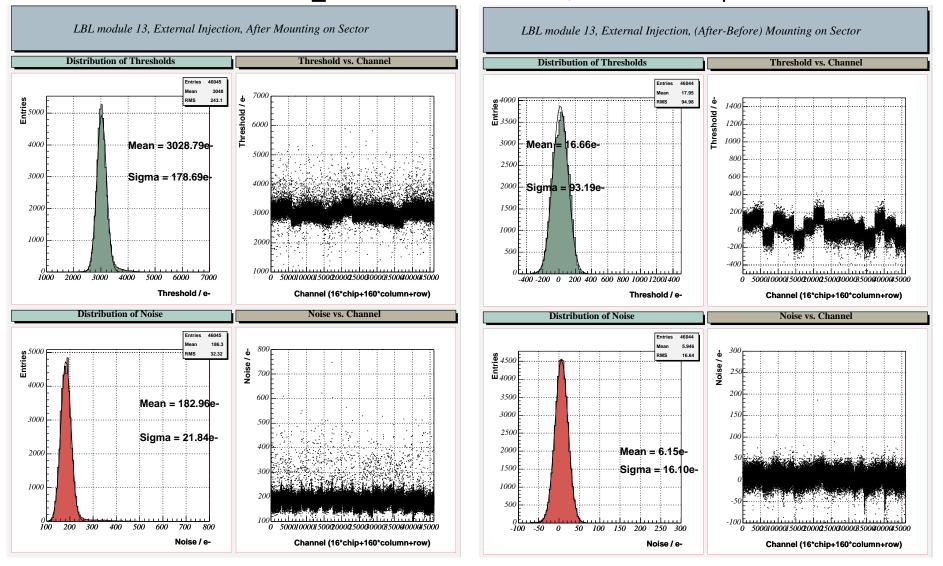
Map of differences for LBL_7:



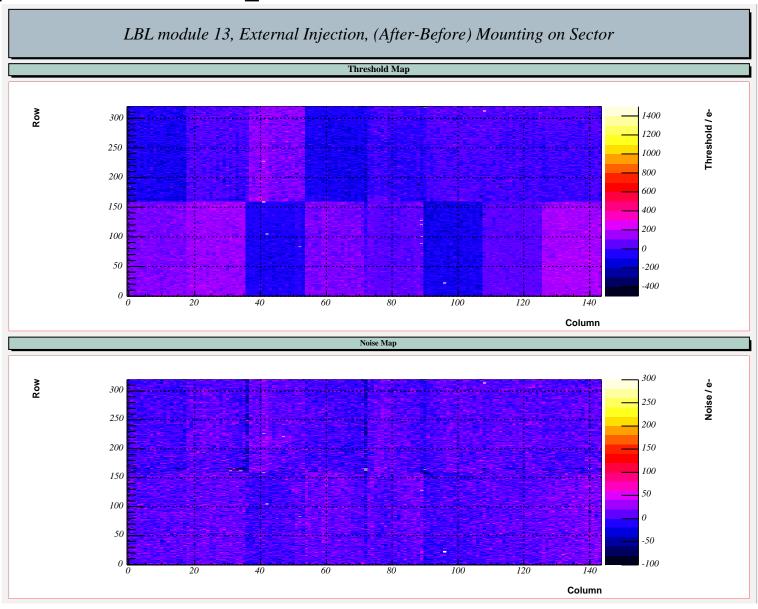
 Major observation is significant bump damage in chip 3. Note chip 10 already showed large region of merged bumps before mounting.

Performance of Six Module Sector

• Compare threshold scans made with single modules in the lab and with modules mounted on sector. LBL_13 shows similar noise, increased dispersion due to ΔT :

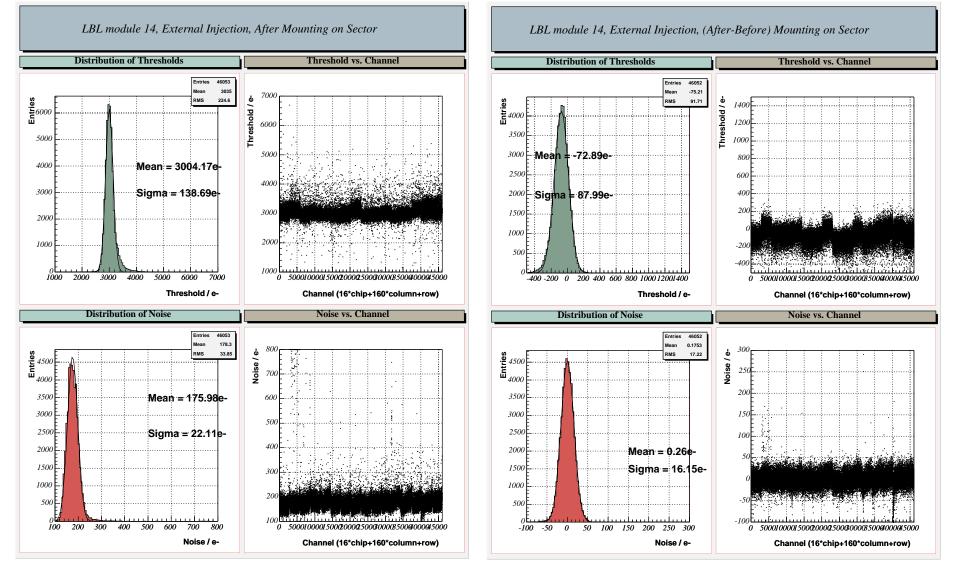


Map of differences for LBL_13:

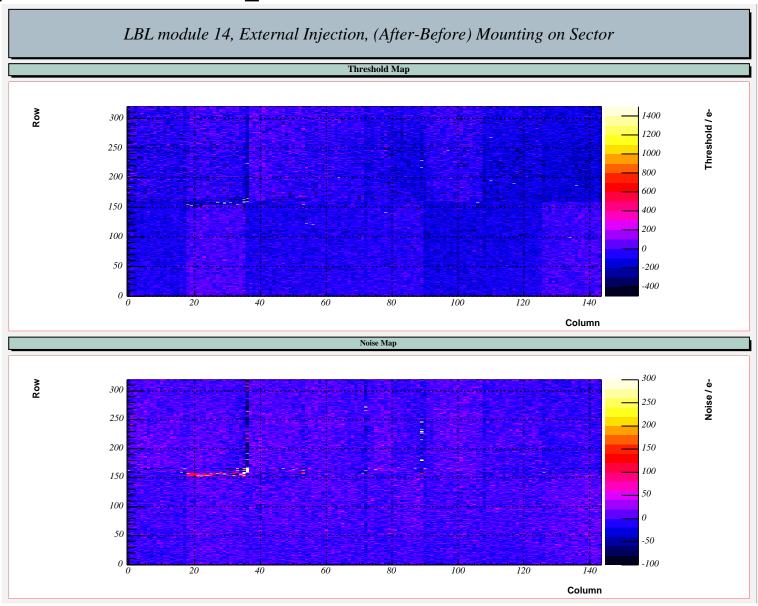


•No significant differences seen.

•Compare threshold scans made with single modules in the lab and with modules mounted on sector. LBL_14 shows similar noise, increased dispersion due to ΔT :

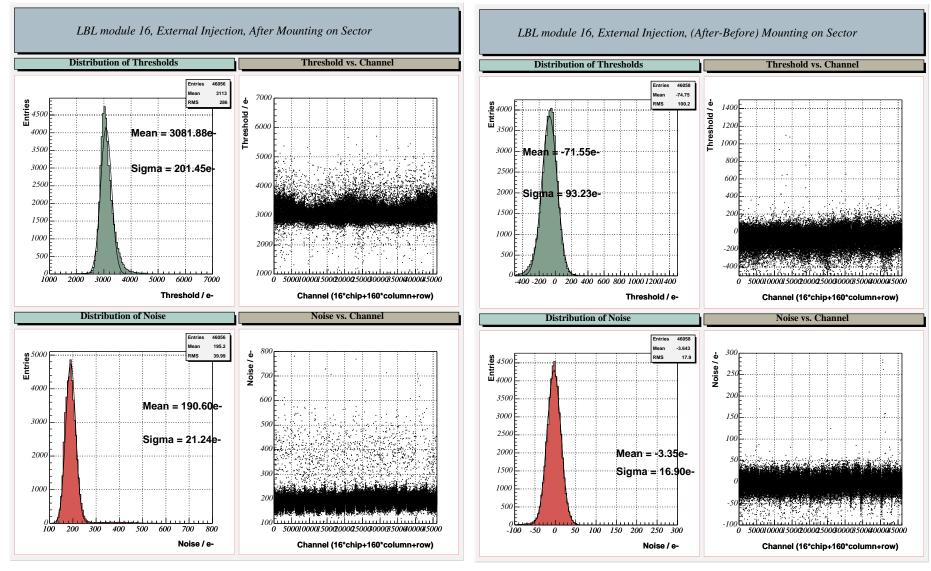


Map of differences for LBL_14:

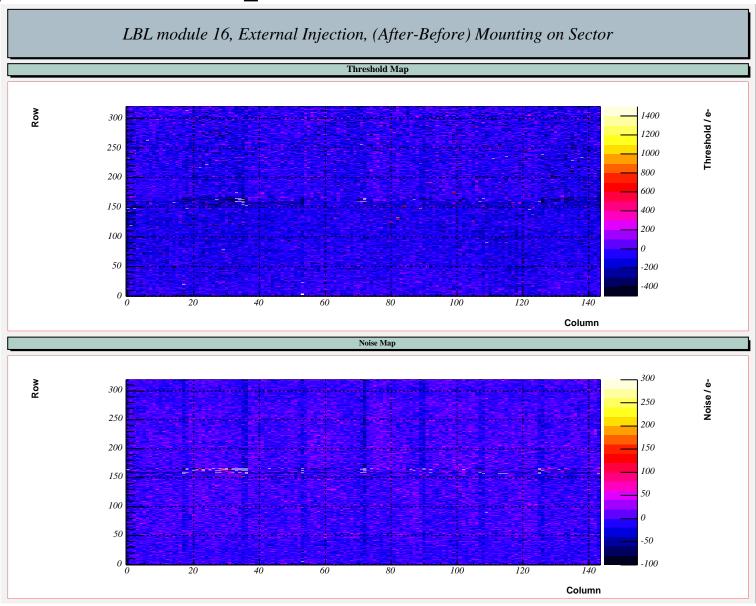


 Only significant shift is in region of chip 1 ganged pixels, which showed very significant merging and poor behavior before mounting on sector.

•Compare threshold scans made with single modules in the lab and with modules mounted on sector. LBL_16 shows similar noise, increased dispersion due to ΔT :



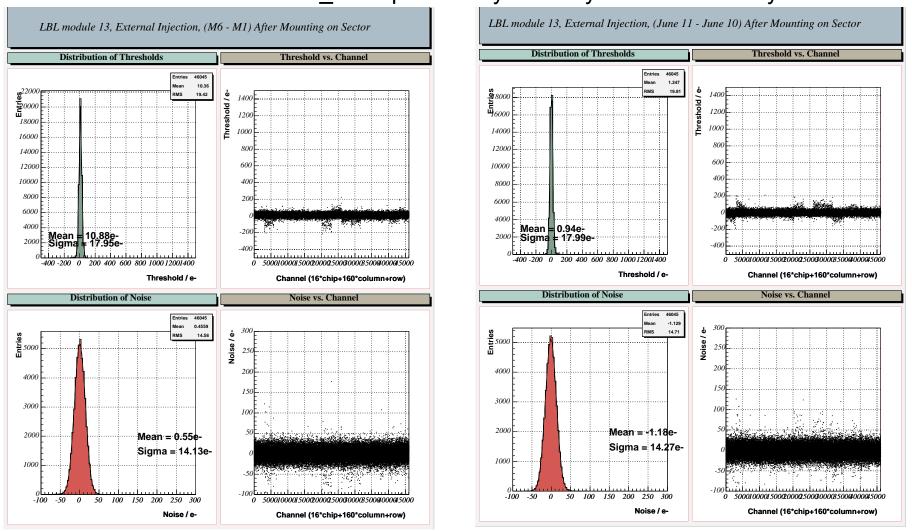
Map of differences for LBL_16:



•No significant differences observed.

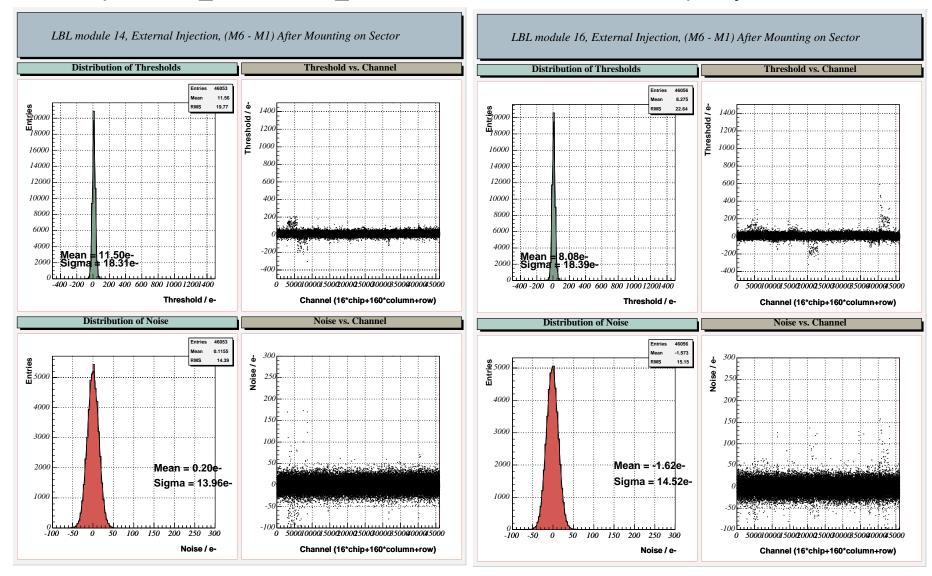
Comparison of Operation with Supply Multiplicity of Six

•Compare LBL_13 behavior on sector with multiplicity one and six. Also, compare two different scans of LBL_13 separated by one day to check stability.



•No significant changes observed. Note all three modules on bottom of sector strobed and triggered simultaneously during these scans.

Compare LBL_14 and LBL_16 behavior on sector with multiplicity one and six.



•No significant changes observed. Note all three modules on bottom of sector strobed and triggered simultaneously during these scans.

Next Steps

Need to make more demanding measurements:

- •Include more complete services model, by using the prototype service panel plus a Type 2 cable made using the real prototype cable from Raydex.
- Get second generation regulator board from Milano, with daughter card, and verify that it works at least as well as the first generation.
- Try to stress the system further by injecting noise in controlled ways into the cooling structure and into the power supplies.
- •Try to implement "bad" grounding schemes to assess the impact.
- Limited ability to make "simultaneous operation" tests with present setup. Using two PCs would help significantly, so implement this for several days.
- Need to proceed to ROD-based system test as soon as this is practical.